

74LVQ138 Low Voltage 1-of-8 Decoder/Demultiplexer

General Description

The LVQ138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three LVQ138 devices or a 1-of-32 decoder using four LVQ138 devices and one inverter.

Features

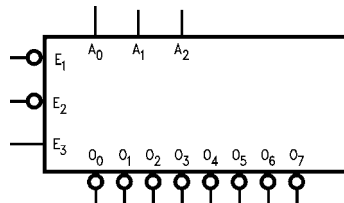
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Guaranteed incident wave switching into 75Ω
- 4kV minimum ESD immunity
- Demultiplexing capability
- Multiple input enable for each expansion
- Active LOW mutually exclusive outputs

Ordering Code:

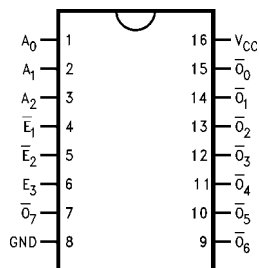
Order Number	Package Number	Package Description
74LVQ138SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVQ138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

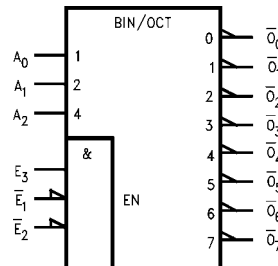
Logic Symbols



IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
A ₀ -A ₂	Address Inputs
\bar{E}_1 - \bar{E}_2	Enable Inputs
E ₃	Enable Input
\bar{O}_0 - \bar{O}_7	Outputs

Functional Description

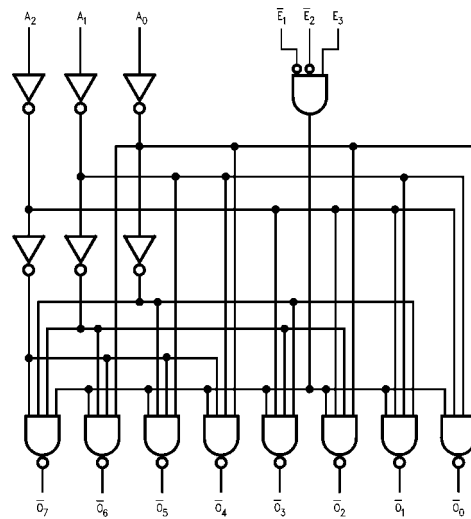
The LVQ138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\bar{O}_0-\bar{O}_7$). The LVQ138 features three Enable inputs, two active-LOW (\bar{E}_1, \bar{E}_2) and one active-HIGH (E_3). All outputs will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LVQ138 devices and one inverter (see Figure 1). The LVQ138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H	H
L	L	H	H	L	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

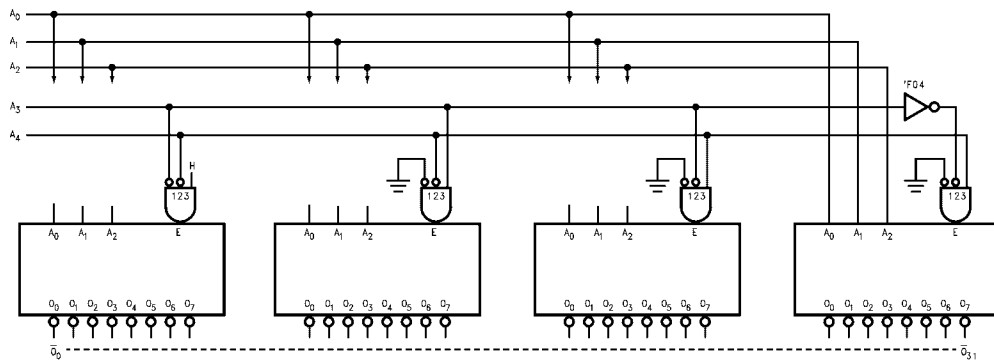


FIGURE 1. Expansion to 1-of-32 Decoding

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 2)				
Supply Voltage (V_{CC})	-0.5V to +7.0V	Supply Voltage (V_{CC})	2.0V to 3.6V			
DC Input Diode Current (I_{IK})		Input Voltage (V_I)	0V to V_{CC}			
$V_I = -0.5V$	-20 mA	Output Voltage (V_O)	0V to V_{CC}			
$V_I = V_{CC} + 0.5V$	+20 mA	Operating Temperature (T_A)	-40°C to +85°C			
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$	Minimum Input Edge Rate ($\Delta V/\Delta t$)				
DC Output Diode Current (I_{OK})		V_{IN} from 0.8V to 2.0V				
$V_O = -0.5V$	-20 mA	V_{CC} @ 3.0V	125 mV/ns			
$V_O = V_{CC} + 0.5V$	+20 mA					
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$					
DC Output Source						
or Sink Current (I_O)	± 50 mA					
DC V_{CC} or Ground Current						
(I_{CC} or I_{GND})	± 200 mA					
Storage Temperature (T_{STG})	-65°C to +150°C					
DC Latch-Up Source or						
Sink Current	± 300 mA					
DC Electrical Characteristics						
Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	V	$I_{OUT} = -50 \mu\text{A}$
		3.0		2.58	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OH} = -12 \text{ mA}$
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	V	$I_{OUT} = 50 \mu\text{A}$
		3.0		0.36	V	$V_{IN} = V_{IL}$ or V_{IH} (Note 3) $I_{OL} = 12 \text{ mA}$
I_{IN}	Maximum Input Leakage Current	3.6		± 0.1	μA	$V_I = V_{CC}$, GND
I_{OLD}	Minimum Dynamic (Note 4)	3.6			mA	$V_{OLD} = 0.8V$ Max (Note 5)
I_{OH}	Output Current	3.6			mA	$V_{OHD} = 2.0V$ Min (Note 5)
I_{CC}	Maximum Quiescent Supply Current	3.6		4.0	μA	$V_{IN} = V_{CC}$ or GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8	V	(Note 6)(Note 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		-0.8	V	(Note 6)(Note 7)
V_{IHD}	Maximum High Level Dynamic Input Voltage	3.3	1.7	2.0	V	(Note 6)(Note 8)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	3.3	1.7	0.8	V	(Note 6)(Note 8)
<p>Note 3: All outputs loaded; thresholds on input associated with output under test.</p> <p>Note 4: Maximum test duration 2.0 ms, one output loaded at a time.</p> <p>Note 5: Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed.</p> <p>Note 6: Worst case package.</p> <p>Note 7: Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V; one output at GND.</p> <p>Note 8: Max number of Data Inputs (n) switching. (n - 1) inputs switching 0V to 3.3V. Input-under-test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), $f = 1 \text{ MHz}$.</p>						

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	2.7	1.5	10.2	18.3	1.5	21.0	ns
	A _n to \overline{O}_n	3.3 ± 0.3	1.5	8.5	13.0	1.5	15.0	
t _{PHL}	Propagation Delay	2.7	1.5	9.6	17.6	1.5	20.0	ns
	A _n to \overline{O}_n	3.3 ± 0.3	1.5	8.0	12.5	1.5	14.0	
t _{PLH}	Propagation Delay	2.7	1.5	13.2	21.0	1.5	23.0	ns
	\overline{E}_1 or \overline{E}_2 to \overline{O}_n	3.3 ± 0.3	1.5	11.0	15.0	1.5	16.0	
t _{PHL}	Propagation Delay	2.7	1.5	11.4	19.0	1.5	21.0	ns
	\overline{E}_1 or \overline{E}_2 to \overline{O}_n	3.3 ± 0.3	1.5	9.5	13.5	1.5	15.0	
t _{PLH}	Propagation Delay	2.7	1.5	13.2	21.8	1.5	23.5	ns
	E ₃ to \overline{O}_n	3.3 ± 0.3	1.5	11.0	15.5	1.5	16.5	
t _{PHL}	Propagation Delay	2.7	1.5	10.2	18.3	1.5	20.0	ns
	E ₃ to \overline{O}_n	3.3 ± 0.3	1.5	8.5	13.0	1.5	14.0	
t _{OSHL}	Output to Output Skew (Note 9)	2.7		1.0	1.5		1.5	ns
t _{OSLH}	Data to Output	3.3 ± 0.3		1.0	1.5		1.5	

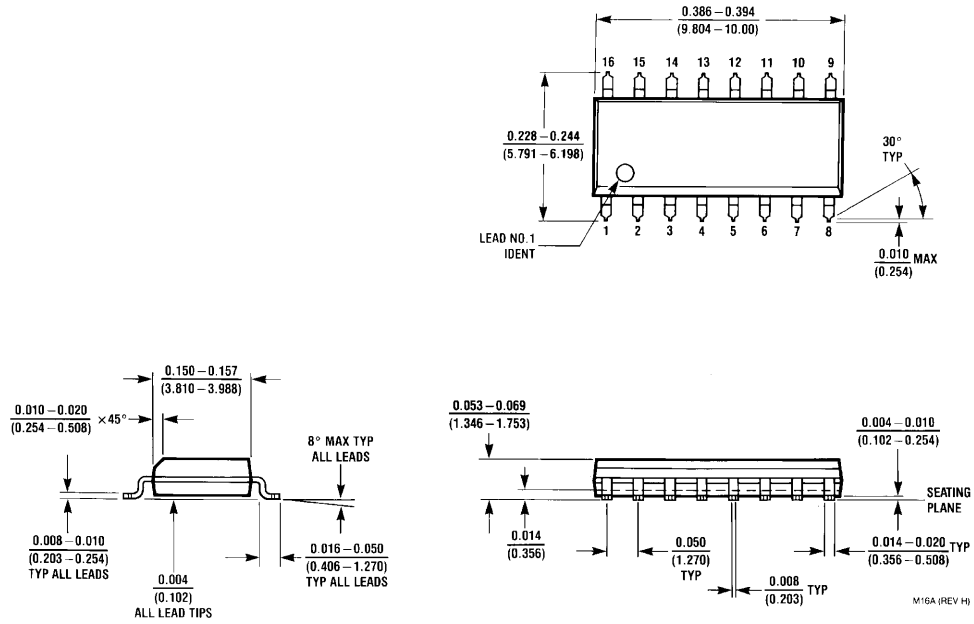
Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = Open
C _{PD} (Note 10)	Power Dissipation Capacitance	45	pF	V _{CC} = 3.3V

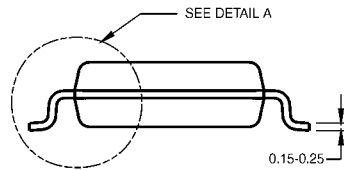
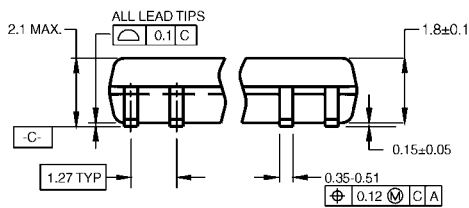
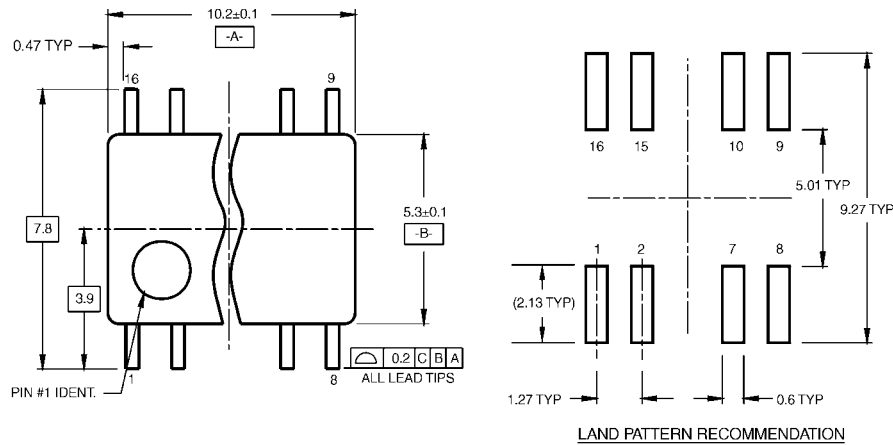
Note 10: C_{PD} is measured at 10 MHz.

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

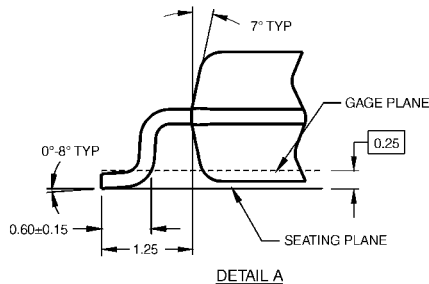
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com